CLAIMS

What is claimed is:

1. A method, comprising:

issuing an advanced load instruction with a first instance of a first destination register;

decoding a test instruction with a second instance of said first destination register where said second instance of said first destination register is decoded as a first source register;

register renaming said first instance of said first destination register and said first source register to a first physical register; and

validating results of said advanced load instruction using said test instruction with said first physical register.

2. The method of claim 1, wherein said test instruction is a load conditional instruction with said second instance of said first destination register.

3. The method of claim 2, further comprising register renaming said second instance of said first destination register to a second physical register.

4. The method of claim 3, wherein said test instruction operates to move contents of said first physical register to said second physical register when said validation indicates said results are valid.

5. The method of claim 1, wherein said test instruction is a speculation check instruction with said second instance of said first destination register.

6. The method of claim 1, wherein said validating includes searching a table for an entry with said first physical register.

7. A processor, comprising:

a decoder to decode a test instruction with a first instance of a first destination register corresponding to a advanced load instruction with a second instance of said first destination register wherein said first instance is decoded as a first source register; and

a register renaming stage to rename said second instance of said first destination register and said first source register to a first physical register.

8. The processor of claim 7, wherein said test instruction is a load conditional instruction.

9. The processor of claim 8, wherein said register renaming stage to rename said first instance of said first destination register to a second physical register.

10. The processor of claim 9, wherein said load conditional instruction operates to move contents of said first physical register to said second physical register when a validation circuit indicates that results of said advanced load instruction are valid.

11. The processor of claim 10, wherein said validation circuit is an advanced load address table.

12. The processor of claim 7, wherein said test instruction is a speculation check instruction.

13. The processor of claim 12, wherein said speculation check instruction is a no-operation when a validation circuit indicates that results of said advanced load instruction are valid.

14. The processor of claim 13, wherein said validation circuit is an advanced load address table.

15. A processor, comprising:

means for issuing an advanced load instruction with a first instance of a first destination register;

means for decoding a test instruction with a second instance of said first destination register where said second instance of said first destination register is decoded as a first source register;

means for register renaming said first instance of said first destination register and said first source register to a first physical register; and

means for validating results of said advanced load instruction using said test instruction with said first physical register.

16. The processor of claim 15, wherein said test instruction is a load conditional instruction with said second instance of said first destination register.

17. The processor of claim 16, further comprising means for register renaming said second instance of said first destination register to a second physical register.

18. The processor of claim 17, wherein said test instruction operates to move contents of said first physical register to said second physical register when said validation indicates said results are valid.

19. The processor of claim 15, wherein said test instruction is a speculation check instruction with said second instance of said first destination register.

20. The processor of claim 15, wherein said means for validating includes a table searchable for an entry with said first physical register.

21. A system, comprising:

a processor including a decoder to decode a test instruction with a first instance of a first destination register corresponding to a advanced load instruction with a second instance of said first destination register wherein said first instance is decoded as a first source register, and a register renaming stage to rename said second instance of said first destination register and said first source register to a first physical register;

an interface to couple said processor to input-output devices; and

an audio input-output circuit coupled to said interface and to said processor.

22. The system of claim 21, wherein said test instruction is a load conditional instruction.

23. The system of claim 22, wherein said register renaming stage to rename said first instance of said first destination register to a second physical register.

24. The system of claim 23, wherein said load conditional instruction operates to move contents of said first physical register to said second physical register when a validation circuit indicates that results of said advanced load instruction are valid.

25. The system of claim 24, wherein said validation circuit is an advanced load address table.

26. The system of claim 21, wherein said test instruction is a speculation check instruction.

27. The system of claim 21, wherein said speculation check instruction is a no-operation when a validation circuit indicates that results of said advanced load instruction are valid.

28. The system of claim 27, wherein said validation circuit is an advanced load address table.